CLAIM LISTING

1. (Original) A method for displaying frames, said method comprising:

fetching a portion of a frame stored in a frame buffer, the portion of the frame stored with a byte order;

storing the portion of the frame in another buffer with the byte order;

fetching a plurality of pixels from the portion of the frame; and

converting the byte order of the plurality of pixels to a predetermined byte order, the byte order being different from the predetermined byte order.

2. (Original) The method of claim 1, further comprising:

decoding the frame; and

storing the frame in the frame buffer with the byte order.

3. (Original) The method of claim 1, wherein the another buffer forms a portion of a display engine.

4. (Original) The method of claim 3, wherein the another buffer forms a portion of a feeder.

5. (Original) The method of claim 1, wherein the predetermined order is selected from a group consisting of big endian byte order and little endian byte order.

6. (Original) The method of claim 1, further comprising:

providing an indicator indicating whether the byte order is different or opposite from the predetermined order.

7. (Original) The method of claim 6, further comprising:

swapping a first one of the plurality of pixels and a second one of the plurality of pixels if the indicator indicates that the byte order is different or opposite from the predetermined order; and

swapping a third one of the plurality of pixels and a fourth one of the plurality of pixels if the indicator indicates that the byte order is different or opposite from the predetermined order.

8. (Original) A system for displaying frames, said system comprising:

a first circuit for fetching a portion of a frame stored in a frame buffer, the portion of the frame being stored with a byte order;

a buffer for storing the portion of the frame with the byte order;

a state machine for fetching a plurality of pixels from the portion of the frame; and

a second circuit for converting the byte order of the plurality of pixels to a predetermined byte order, the byte order being different from the predetermined byte order.

9. (Original) The system of claim 8, further comprising:

a video decoder for decoding the frame; and

the frame buffer for storing the frame with the byte order.

10. (Original) The system of claim 8, wherein the first circuit comprises an input data write unit.

11. (Original) The system of claim 8, wherein the buffer forms a portion of a display engine.

12. (Original) The system of claim 10, wherein the buffer forms a portion of a feeder.

13. (Original) The system of claim 8, wherein the predetermined order is selected from a group consisting of big endian byte order and little endian byte order.

14. (Original) The system of claim 8, wherein the state machine provides an indicator indicating whether the byte order is different or opposite from the predetermined order to the second circuit.

15. (Original) The system of claim 14, wherein the second circuit further comprises:

a first multiplexer for selecting one of a first one of the plurality of pixels and a second one of the plurality of pixels;

a second multiplexer for selecting another of the first one of the plurality of pixels and the second one of the plurality of pixels, from the first multiplexer;

a third multiplexer for selecting one of a third one of the plurality of pixels and a fourth one of the plurality of pixels;

a fourth multiplexer for selecting another of the third one of the plurality of pixels and the fourth one of the plurality of pixels, from the third multiplexer;

a fifth multiplexer for multiplexing outputs from the first multiplexer, the second multiplexer, the third multiplexer, and fourth multiplexer; and

the selections of the first multiplexer, the second multiplexer, the third multiplexer, and the fourth multiplexer being controlled by the indicator provided by the state machine.

16. (Original) A method for displaying frames, said method comprising:

fetching a portion of a frame stored in a frame buffer, the portion of the frame being stored with a pixel order;

storing the portion of the frame in another buffer with the pixel order;

fetching a plurality of pixels from the portion of the frame; and

converting the pixel order of the plurality of pixels to a predetermined pixel order.

17. (Currently Amended) The method of claim 16, further comprising:

decoding the frame; and

storing the frame in the frame buffer with the ~~byte~~ pixel order.

18. (Original) The method of claim 16, wherein the another buffer forms a portion of a display engine.

19. (Original) The method of claim 18, wherein the another buffer forms a portion of a feeder.

20. (Original) The method of claim 16, further comprising:

rearranging the plurality of pixels in plurality of different pixel orders;

receiving an indicator indicating the pixel order; and

selecting the pixels rearranged in one of the plurality of different pixel orders based on the indicator indicating the pixel order.

21. (Original) A system for displaying frames, said system comprising:

an input data write unit for fetching a portion of a frame stored in a frame buffer, the portion of the frame being stored with a pixel order;

a buffer for storing the portion of the frame with the pixel order;

a buffer read state machine for fetching a plurality of pixels from the portion of the frame; and

a circuit for converting the pixel order of the plurality of pixels to a predetermined pixel order.

22. (Currently Amended) The system of claim 21, further comprising:

a decoder for decoding the frame; and

the frame buffer for storing the frame with the ~~byte~~ pixel order.

23. (Original) The system of claim of claim 21, wherein the buffer forms a portion of a display engine.

24. (Original) The system of claim 23, wherein the buffer forms a portion of a feeder.

25. (Original) The system of claim 21, wherein the circuit forms a portion of a pixel feeder.

26. (Currently Amended) The system of claim 21, wherein the circuit further comprises:

a demultiplexer for separating the plurality of pixels;

a plurality of multiplexers for combining the separated plurality of pixels in a corresponding plurality of pixel orders; and

another multiplexer for selecting an output from one of the plurality of multiplexers, based on an indicator indicating the pixel order provided by the ~~state machine~~ circuit.

27. (Original) A method for displaying frames, said method comprising:

fetching a portion of a frame stored in a frame buffer;

storing the portion of the frame in another buffer;

fetching a plurality of pixels from the portion of the frame;

storing luma pixels in a luma pixel register, if the plurality of pixels comprise luma pixels; and

storing chroma pixels in a chroma pixel register, if the plurality of pixels comprise chroma pixels.

28. (Original) The method of claim 27, further comprising:

decoding the frame; and

storing the frame in the frame buffer.

29. (Original) The method of claim 27, wherein the another buffer forms a portion of a display engine.

30. (Original) The method of claim 29, wherein the another buffer forms a portion of a feeder.

31. (Original) The method of claim 27, wherein storing the luma pixels in the luma pixel register further comprises:

receiving the plurality of pixels; and

providing the luma pixels to the luma pixel register, if the plurality of pixels comprise luma pixels.

32. (Original) The method of claim 27, wherein storing the luma pixels in the luma pixel register further comprises:

receiving the plurality of pixels over a first path;

receiving a portion of the plurality of pixels over a second path;

selecting the plurality of pixels from the first path, if all of the plurality of pixels are luma pixels; and

selecting the portion of the plurality of pixels from the second path, if a portion of the plurality of pixels are luma pixels and another portion of the plurality of pixels are chroma pixels.

33. (Original) The method of claim 27, wherein storing chroma pixels in the chroma pixel register further comprises:

receiving the plurality of pixels; and

providing the chroma pixels to the chroma pixel register, if the plurality of pixels comprise chroma pixels.

34. (Cancelled)

35. (Original) The method of claim 27, wherein storing chroma pixels in the chroma pixel register further comprises:

receiving the plurality of pixels;

providing chroma red pixels to a chroma red pixel register, if the plurality of pixels comprise chroma red pixels; and

providing chroma blue pixels to a chroma blue pixel register, if the plurality of pixels comprise chroma blue pixels.

36. (Original) The method of claim 27, wherein storing the chroma pixels in the chroma pixel register further comprises:

receiving the plurality of pixels over a first path;

receiving a portion of the plurality of pixels over a second path;

selecting the plurality of pixels from the first path, if all of the plurality of pixels are chroma pixels; and

selecting the portion of the plurality of pixels from the second path, if a portion of the plurality of pixels

are chroma pixels and another portion of the plurality of pixels are luma pixels.

37. (Original) The method of claim 36, further comprising:

storing at least one of the plurality of pixels in a chroma red pixel register, if the plurality of pixels are selected;

storing at least one of the plurality of pixels in a chroma blue pixel register, if the plurality of pixels are selected;

storing at least one of the pixels from the portion of the plurality of pixels from the second path in the chroma red pixel register, if the portion of the plurality of pixels are selected; and

storing at least one of the pixels from the portion of the plurality of pixels from the second path in the chroma blue pixel register, if the portion of the plurality of pixels are selected.

38. (Original) A system for displaying frames, said system comprising:

a first circuit for fetching a portion of a frame stored in a frame buffer;

a buffer for storing the portion of the frame;

a state machine for fetching a plurality of pixels from the portion of the frame;

a luma pixel register for storing luma pixels, if the plurality of pixels comprise luma pixels; and

a chroma pixel register for storing chroma pixels, if the plurality of pixels comprise chroma pixels.

39. (Original) The system of claim 38, further comprising:

a video decoder for decoding the frame; and

the frame buffer for storing the frame.

40. (Original) The system of claim 38, wherein the buffer forms a portion of a display engine.

41. (Original) The system of claim 40, wherein the buffer forms a portion of a feeder.

42. (Original) The system of claim 38, further comprising:

a first multiplexer for receiving a first portion of the plurality of pixels over a first path, and for receiving a second portion of the plurality of pixels over a second path, the first multiplexer associated with a first portion of the luma pixel register;

a second multiplexer for receiving a remainder of the plurality of pixels from the first portion of the plurality of pixels over a first path, and for receiving the second portion of the plurality of pixels, the second multiplexer associated with a second portion of the luma pixel register; and

the first multiplexer provides the portion of the plurality of pixels to the first portion of the luma pixel registers and the second multiplexer provides the remainder of the plurality of the pixels to the second portion of the luma pixel register if the portion of the plurality of pixels and the remainder of the plurality of pixels comprise luma pixels;

the state machine selects one of the first multiplexer and the second multiplexer, the selected one of the multiplexers providing the second portion of the pixels to the associated portion of the luma pixel register, if the plurality of pixels comprise luma and chroma pixels.

43. (Original) The system of claim 38, further comprising:

a first multiplexer for receiving a first portion of the plurality of pixels over a first path, and for receiving a second portion of the plurality of pixels over a second path, the first multiplexer associated with a first portion of the chroma pixel register;

a second multiplexer for receiving a remainder of the plurality of pixels from the first portion of the plurality of pixels over a first path, and for receiving the second portion of the plurality of pixels, the second multiplexer associated with a second portion of the chroma pixel register; and

the first multiplexer provides the portion of the plurality of pixels to the first portion of the luma pixel registers and the second multiplexer provides the remainder of the plurality of the pixels to the second portion of the luma pixel register if the portion of the plurality of pixels and the remainder of the plurality of pixels comprise chroma pixels;

the state machine selects one of the first multiplexer and the second multiplexer, the selected one of the multiplexers providing the second portion of the plurality of pixels to the associated portion of the luma pixel register, if the plurality of pixels comprise luma and chroma pixels.